Lab #2: Cell layout
ECEn 451
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In this lab you will use the Cadence tools to create layouts for the simple cell you created for the last lab. You will verify that the layout and the schematic match and that there are no design rule violations in the layout.

For this lab, you should work in the same team you used for Lab #1. First, create a stick diagram of the layout. Then create the layout for the cell you chose for Lab #1. To make it easier to create this layout, I have provided a standard cell template file on Blackboard. To place it in your cell library, change to the library directory and untar the template with:

tar -xzvf template.tgz

This will create the standard cell layout template cell in your library. You can then copy it to begin the layout for your cell. The template contains the wells, Vdd and GND rails with well taps, nselect, and pselect areas as described in the layout tutorial. You should resize its elements horizontally as necessary for your cell, but be sure not to change the vertical dimensions.

Be particularly careful to:

1) Match the size of the transistors in the layout with that in the schematic!
2) Make sure that the order of transistors in each leg is the same in the schematic and in the layout.

In either case, the LVS tool will report errors.

Deliverables

Turn in the following:

1. A stick diagram of the cell layout.
2. A color plot of the layout.
3. A screen capture of the DRC output (with no errors) (unfortunately, we haven't figured out how to create a logfile)
4. The LVS output file (with no errors)

Be aware that if you choose to work in a team that you are both responsible for knowing how to use all the tools. There will be exam questions which cover tool usage.