Homework #10: Circuit families
ECEn 451
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In all of these problems, when the book says λ, assume that they mean a multiplier of the unit transistor width (since, after all, if it meant the process lambda, you'd have to know the design rules to figure out the unit transistor width!) Thus the unit inverter presents 3 λ of transistor width and therefore 3C capacitance.

1. Problem 9.1, parts a and b

2. Problem 9.11

3. Problem 9.12

4. Problem 9.18

5. Problem 9.20 - Use a pullup which is 1/4 the strength of the pulldown. (The strange statement about the parasitic delay is really a hint as to what the pullup/pulldown strength ratio should be ... it implies that when n-transistors have a width of 4, p-transistors have a width of 2.) Note that the rising and falling delays will be different and must both be analyzed! Note also that your solution will be comprised of multiple gates, like the big "determine the best circuit architecture" problems we did using logical effort.