Homework #14: Power and Clocks
ECEn 451
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1. Problem 4.27

2. Problem 4.28

3. Suppose :
   - The Vdd and GND busses for a row of standard cells are 1 um wide and 200 um long in metal 1 (Rsq = 0.08 ohms/sq)
   - Vdd is 1.5V.
   - Each standard cell drives 14 fF at an edge rate of 150ps and is 20um wide.

   How much does Vdd droop at the end of the bus?

4. How much on-chip bypass capacitance would you need to add to prevent a supply voltage droop of more than 100mV when there is a 30A current change in one clock cycle and the clock frequency is 2GHz? Assume that there are 100M transistors and the average transistor gate capacitance is 1.4 fF.

5. You are designing a PCI bus device to operate at 66 MHz. Your design has the following characteristics:
   - The input pad buffers for both data and clock have a delay of 250 ps.
   - The clock tree distributes the clock signal to flops with 400ps delay and zero skew.
   - The shortest path between an input pad and any flop is 100 ps.
   - T_{hold} for a flop is 30 ps.

   a) If there is no PLL, what hold time would you measure for an input signal? (In other words, how long does an input signal have to be held after the external clock's arrival to prevent hold time violations at the flops inside the chip?

   b) If there were a PLL, how much delay must be in the PLL's feedback path to ensure that the measured hold time for input signals is -20ps?