Homework 6: RC delays
ECEn 451
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Answer the following questions (assuming that relative mobility is 2):

1. Problem 4.1 (Hint: read the problem carefully; there is no sharing of diffusion in this layout, even between series transistors! Also, note that the load is multiple NOR gates, not an inverter.)

2. Problem 4.2. Use a layout which minimizes diffusion capacitance by sharing all diffusion nodes possible. However, ignore the sentence that says to budget only half the capacitance for uncontacted shared nodes; instead, do what we have done in class and budget contacted and uncontacted nodes alike.

3. Redo problem 4.2 with p-mos transistors that are three times as wide of those of 4.2. (use the same stick diagram; you don't have to draw it again. Use *h* instances of the new NOR gate as the load.)

4. Redo problem 4.2 with n-mos transistors that are three times as wide of those of 4.2. (use the same stick diagram; you don't have to draw it again. use *h* instances of the new NOR gate as the load.)

5. Why do you need to use at least two gates in series as the load when characterizing a gate? (i.e., why do you set up characterization with the gate under test followed by an inverter followed by an inverter?)