Homework #9: Wires and noise
ECEn 451
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1. Problem 6.2

2. Problem 6.3. Assume that the unit transistor is 3 lambda wide.

3. Assume that two wires run next to each other with 0.2 pF of capacitance between them and that wire 1 has capacitance of 0.1 pF to ground while wire 2 has a capacitance of 0.5 pF to ground. Assume further that wire 1 is driven by a 32x gate, wire 2 is driven by a 2x gate, and the effective output resistance of a 1x gate is 9 KΩ. When wire 1 switches from ground to Vdd while wire 2 is held low, what is the maximum amount of noise on wire 2?

4. Repeat problem 3 if wire 2 is undriven.

Solve the following problems for an 180 nm 6-layer process having the following measured parameters:

- Effective output resistance of a minimum length transistor = 2.5KΩ * µm
- Gate capacitance of a minimum length transistor = 2 fF / µm.
- Relative mobility = 2
- Width of a minimum width metal 4 wire = 450 nm.
- Sheet resistance of metal 4 = 0.03 Ω

Let the unit inverter's nMOS transistor have gate width = 3 lambda = 270 nm
You may ignore diffusion parasitics.

5. Assume a minimum width wire route of 7mm in layer 4 metal with Cw = 210 aF/µm . How many repeaters should be inserted for minimum delay?

6. How large should the repeaters be (in terms of multiples of the unit inverter) and what will the delay be once repeaters are inserted?