

Lab 3: Cell Characterization
ECEn 451
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In this lab you will use the Cadence tools to characterize a standard cell through simulation. You are to provide the following information **for each input pin**:

1. Its total gate capacitance, assuming that $C_{\text{gox}} = 1 \text{ fF} / \mu\text{m}^2$
2. The intrinsic delay through the gate when that input rises and when it falls, based upon 50%-50% delay
3. The effective output resistance through the gate when the input rises and when it falls, based upon 50%-50% delay

The lab tarfile `LabCharFiles.tgz` should be unpacked in a library which has the AMI12 tech library attached. The tarfile contains two cells: the unit inverter (INV_1x), and an AOI21_1x gate. You are to characterize the AOI21_1x gate.

Your characterization circuit should present inputs through a series of two unit inverters to shape the input waveform and should use a load of either two unit inverters in series to reduce the Miller effect or four copies of such a series. The edge time of the waveform generator should be set to 100ps. Use the calculation methods given in class, **not** those on the tutorial web pages. Measure both rise and fall delays for each load condition. Plot the rise delays and fall delays as a function of load, where load is specified in units of capacitance and is calculated from the unit inverter's layout. Find the y-intercept and slope of each line; the y-intercept is the intrinsic delay (i.e. the delay with no load) and the slope is the effective resistance.

The Cadence tutorial web page lists a tutorial which you should read. **Rely upon it only for instructions about how to run tools, as your assignment is quite different from the activities described in the tutorial, particularly with respect to input waveforms and loads..** Be sure to set both the INV_1x and AOI21_1x to use the analog_extracted views. (Something else that wasn't mentioned in the tutorial: how do you get analog_extracted views? In this particular case, I've given them to you. For future reference, if you want to generate them, you do it from the LVS window with the "Build Analog" button.)

Deliverables

Turn in the following:

1. A table which indicates the items listed above for each pin.
2. A plot (not a screen capture!) of one of your simulations, with input and output marked and showing at least one rise and fall of the input.
3. The complete schematics describing the simulation plotted in #3 (but you do not need to include schematics for INV_1x and AOI21_1x)

Be aware that if you choose to work in a team that you are both responsible for knowing how to use all the tools. There will be exam questions which cover tool usage.