Lab #4: Noise
ECEn 451
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In this lab you will use the Cadence tools to analyze how coupling noise on wires affects dynamic logic. There are four parts.

The lab 4 tarball on Blackboard includes a dynamic inverter to be analyzed, the 1x inverter we used before, and a 32x inverter for creating sharp aggressor edges.

**NOTE: For this lab, you will not create a config view for the simulator. Instead, you'll just simulate from the schematics. This is a common thing to do when you don't have layouts yet and are still exploring the design space. We used a config view in the last lab because we wanted to characterize a cell given a particular layout.**

**NOTE 2: Look at the deliverables closely as you will want to print out results at intermediate stages of your work.**

<u>Part I: No noise</u>
Set up a characterization environment by creating a new schematic and instantiating the provided elements as you did in lab 3. In this case, we will characterize the dinv_1x cell for noise. This cell is a footed dynamic inverter. Use the following setup.

1. As is customary, drive the data input (pin A) of the cell with a pair of 1x static inverters in series.
2. Do likewise for the clock input (pin CLK).
3. Load the footed dynamic inverter with a pair of 1x static inverters in series
4. Use a pulse generator to drive the clock input path. Use a 40ns period, 20ns pulse width, and 2ns rise and fall times.
5. Tie off the data input path to Vdd (so that the dynamic inverter's output during evaluation should fall.)

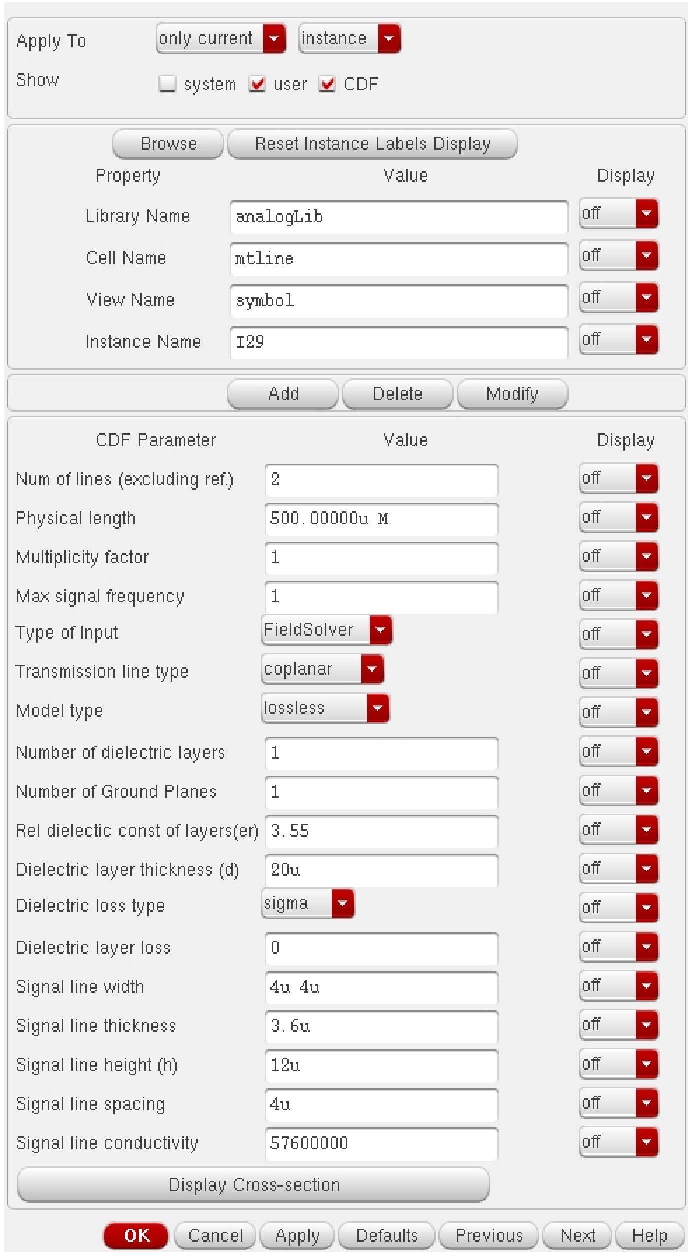
Launch and configure the Analog Design Environment as in Lab 3 and simulate this configuration for 200ns to ensure that your dynamic inverter actually works. You'll see the output rise when the clock is low and fall when it is high. The output rising edge will be considerably slower and “rounder” than the falling edge.

**Print a plot of the input, clock, and output waveforms.**

<u>Part II: Adding noise</u>
What we're going to measure is how coupling noise on the input to a dynamic gate can affect the output. During the evaluate stage, if the input is low, the output is supposed to remain floating high. Any noise on the input which pushes it above Vt will cause the nmos transistor to turn on momentarily and partially discharge the output node, resulting in a bad output level.

Change your schematic in the following manner:

1. Tie off the data input path to GND now. (So what you want to see on the output is a steady high value.)
2. Add a 32x inverter whose input is a pulse generator with a period of 80ns and an initial delay of 10ns. This inverter's output will be the aggresssor signal. The initial delay ensures that the output of the inverter changes during the evaluation portion of the clock cycle.
3. Instantiate a transmission line to model the coupling between the wires. The transmission line is the *mtline* cell from the *analogLib* library*passives* category.
4. Set the transmission line's parameters to the following:




**NOTE: You will not see exactly the same dialog box when you first open the cell's parameter window. Most of the options won't appear until after you set the "Type of input" to "FieldSolver". Also, the symbol may not have the right number of terminals until you set all the parameters properly and press OK.**

What this dialog box is doing is describing the geometry of the wires and the characteristics of the materials. Spectre contains a field solver which uses these parameters to determine the coupling, without you having to figure out the capacitances. Very cool! In this case, we've said that there will be two wires in the same plane which run next to each other for 500 microns. Each wire is 4 microns wide and 3.6 microns tall with 4 micron spacing between them. The wires are 12 microns above the "ground plane" (essentially the substrate). The dielectric constant of the oxide is 3.55 and the conductivity of the wires is 5,760,000 siemens. (These last two process numbers may not be exact for AMI12, but they're the right orders of magnitude.) If you press the "Display Cross-section" button, you'll get a popup window which shows a cross-section of the wire geometry.

5. The transmission line box will have six terminals. Connect the upper two between the last “data-driving” inverter and the dynamic inverter's input pin. Connect the middle two between the output of the 32x inverter and a load consisting of two 1x inverters in series. Connect the bottom two to ground.

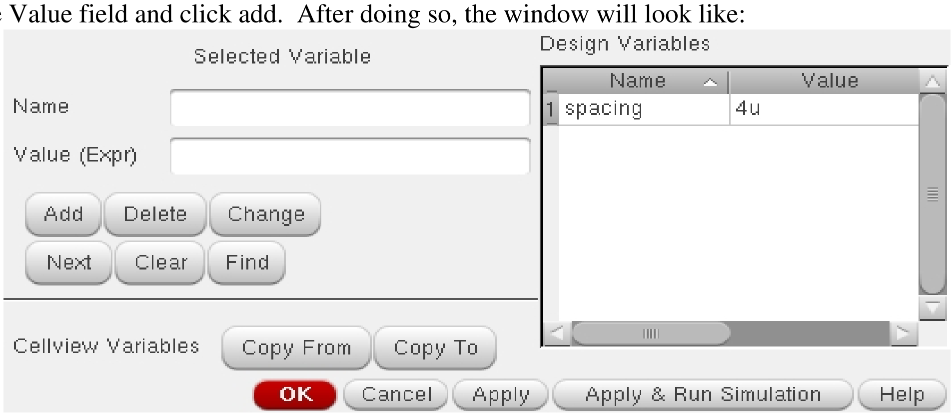
Now, simulate the design. You should see a lot of noise (up to two volts) appearing on the input pin of the inverter and the output of the inverter dropping to nearly four volts.

**Print a plot of the input, clock, and output waveforms.**

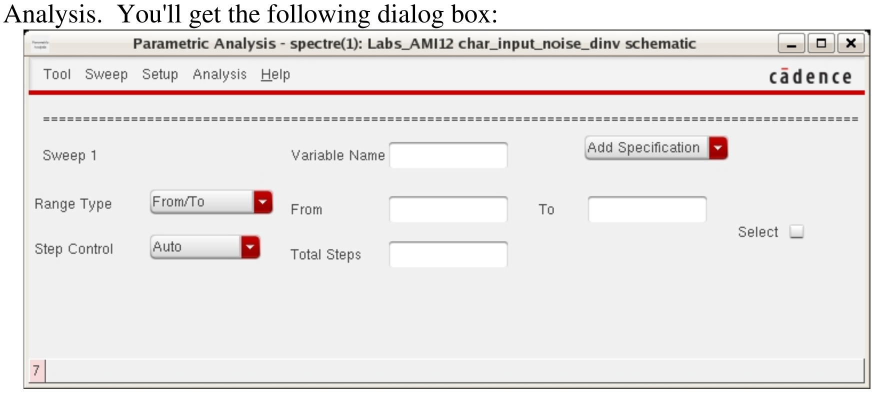
Part III: Characterizing noise vs. wire spacing.

In this part we'll characterize the amount of noise you get as the wire spacing changes. The goal is to obtain a graph of noise vs. spacing. The kind of analysis we're doing is called *parametric analysis* -- you change one parameter in the design and see what the effects are. To set up this parametric analysis, you have to add a parameter to the design:

1. In the schematic, open the properties of the transmission line and change the “Signal line spacing” property to read “spacing”. You may get a warning about how the value should be a number in the virtuoso window. Ignore it.
2. In the Analog Design Environment (ADE) window, select Variables->Edit. Enter “spacing” in the Name field and 4u in the Value field and click add. After doing so, the window will look like:



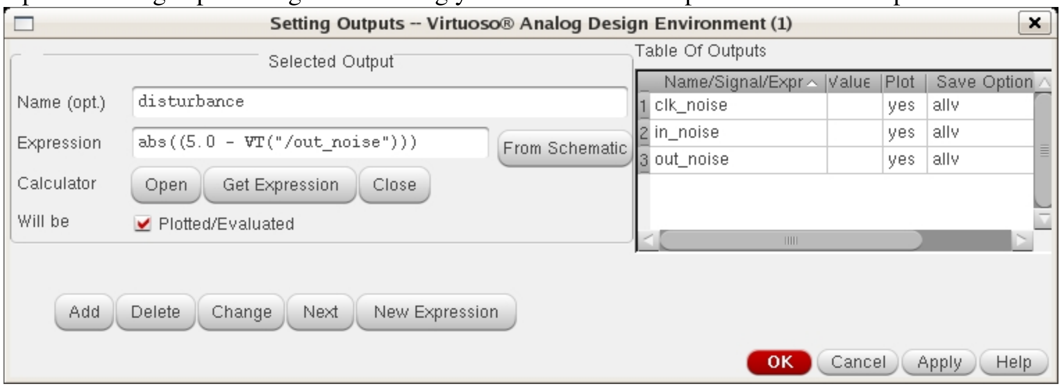

Now, you need to tell the simulator to do a parametric analysis. To do so, go to the ADE window and select Tools -> Parametric Analysis. You'll get the following dialog box:




Enter spacing into the Variable Name box. Se the range from 4u to 40u. Set the total steps to 10 and click the select button. This tells ADE to run 10 simulations, with different spacing in each one: 4u, 8u, 12u, ... up to 40u..

Run the simulations by selecting Analysis->Start in the Parametric Analysis window. It will take a few moments! You'll see the waveforms of all the simulations on the same graph. To see each family of waveforms in a different strip click on the Trace menu and verify that the "Strip by Family" box is selected; then select the "Strip Chart Mode" button from the toolbar.

Now, create a graph of maximum amount of output disturbance vs. spacing.  To do this, go to the ADE window and select Outputs->Setup.  This brings up a dialog box allowing you to create new outputs which are computed formulas:




**NOTE: the picture above shows what the box would look like just before pressing "Add" as described below.  (your output signal names on the right may vary...)**

Set up the measurement of the disturbance by doing the following:

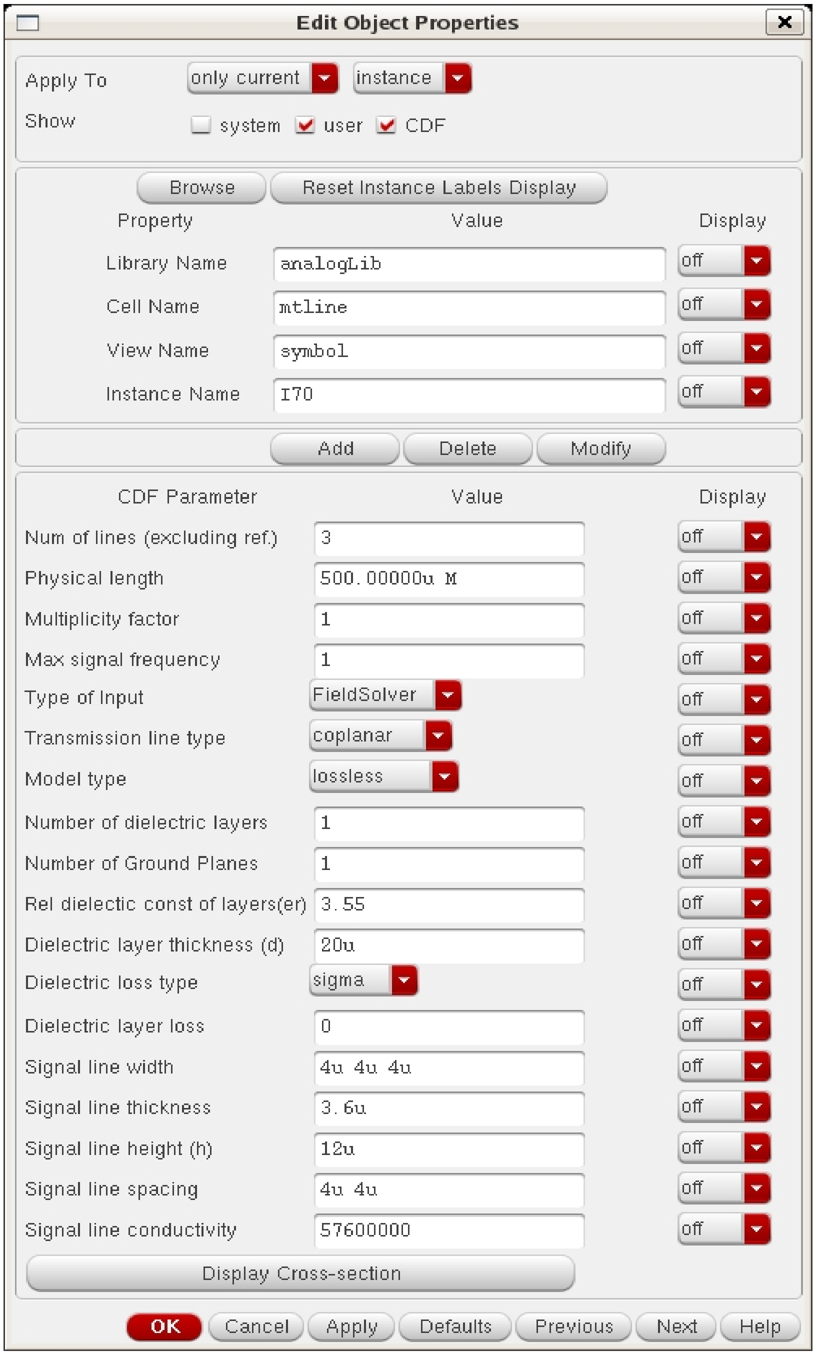
1. Press the "Open" button to open the calculator.
2. Select vt
3. Select the output of the dynamic inverter on the schematic and hit escape.  Make sure that the expression shown in the calculator is VT("/name-of-the-dynamic-output-node")
4. Go back to the "Setting Outputs" window (don't close the calculator)
5. Type "disturbance" in the Name field; this will name you're expression.
6. Press "Get Expression" to get the current expression from the calculator.
7. Edit the expression (in the Setting Outputs window) to be:
   `ymax(abs(5.0 -VT("/output_node_of_the_dynamic_inverter")))`.
   **At this point, the dialog box would look like the picture above.**
8. Click Add and then OK.

Now, re-run the parametric simulations.  Besides the waveform graphs, you'll now have a graph plotting the disturbance vs. the spacing.

**Print a plot of the input, clock, and output waveforms. and the disturbance-vs.-spacing graph.  When printing, select *All Subwindows* to print both the waveform and graph.  Also, print the schematic of your characterization environment.**

Part IV

In this final part, you will examine the impact of shielding on the wires. Change the mtwire element to have the following properties:




This cross section has three wires spaced 4u apart. (Press Display Cross-section to see this.) We'll put the victim on the leftmost wire and the aggressor on the rightmost wire. The middle wire will be tied to ground to act as a shield.

You'll see that the symbol now has eight terminals. The upper terminals are used for the input of the dynamic inverter, as before. The second set of terminals from the top should be attached to ground on the left and nothing on the right. The aggressor wire and its load should be attached to the third set of terminals. The bottom terminals connect to ground.

Run the simulation (not a parametric simulation this time) and see how well the shield worked. The “disturbance” output variable from part III should still be valid and will appear in the ADE window with a numeric value representing the measurement of the disturbance with the shielding in place

**Print a plot of the input, clock, and output waveforms.**

Deliverables

Provide the following in your report:

1. Names of team members (up to two). You may choose your team members or may choose to work individually.
2. A plot showing the dynamic inverter's input, clock, and output waveforms in Part I.
3. A plot showing the dynamic inverter's input, clock, and output waveforms in Part II.
4. A plot showing both the dynamic inverter's input, clock, and output waveform as the spacing is changed and the disturbance vs. spacing graph in part III
5. Schematics of the environment you used in Part III.
6. A plot showing the dynamic inverter's input, clock, and output waveforms in Part IV.

**You must provide hard-copy; electronic submissions will not be accepted.**

Be aware that if you choose to work in a team that you are both responsible for knowing how to use all the tools. There will be exam questions which cover tool usage.