

Lab #5: Sequential circuit element design
ECEn 451
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In this lab you will use the Cadence tools to design a sequential circuit element.

NOTE: For this lab you will not create a config view for the simulator because we do not have layouts for the cell you are designing.

You are to provide a transistor-level design of one of the following circuits:

1. A pulsed latch with an *internal* pulse generator. Variants of the designs in Figure 7.22 are acceptable, as would be a design of your own invention, so long as it functions as a pulsed latch. The output node should be staticized (i.e. not a dynamic node)
2. A Partovi pulsed latch with a staticized output - Section 7.3.3
3. A Klass semi-dynamic flop (note: this one is tricky, but might be fun) - Section 7.3.7

Use the following names for your pins: D, CLK, and Q.

Also, you need to generate a “symbol” view of your cell so that you can instantiate it in a test and/or characterization environment. To do this, open the schematic and select Create-> Cellview -> From Cellview. Most of the fields should be filled in for you already; make sure that the library and cell name are correct and the “To View Name” is “symbol”. Then press OK. You'll be given another dialog box called “Symbol Generation Options”. Make sure that the left pins line lists D and CLK and the right pins line lists Q. Then press OK. The Symbol Editor will open with a newly created symbol view for your cell. It's not very interesting (just a box), but it will do. You can make it prettier if you like; if not, simply close the symbol editor.

You do not need to do layout.

Set up a test environment by creating a new schematic and instantiating your latch/flop and the provided elements as you did in labs 3 and 4. In this case, you'll be characterizing your new cell. Use the following setup:

1. As is customary, drive the data input (pin D) of the cell with a pair of 1x static inverters in series.
2. Do likewise for the clock input (pin CLK)
3. Load the Q output with four parallel pairs of 1x static inverters in series. (As in lab 3)
4. Use a pulse generator to drive the clock input path. Use a 40ns period, 20ns pulse width, 2 ns rise and fall times, and 12ns delay time. (This delay time is chosen to ensure that the data doesn't transition near the clock for the moment.)
5. Use a pulse generator to drive the data input path. Use a 80ns period, 40ns pulse width, and 2ns rise and fall times, and 0 delay time.
6. Label the wires connected to the CLK, D, and Q pins as “CLKin”, “Din”, and “Qout”.

Launch and configure the Analog Design Environment as in Lab 4 and simulate this configuration for 400ns. You should see the Q output changing some time after the clock edge. If you do not see the proper behavior, double-check your configuration. If it still doesn't work, you'll need to debug your design. Common errors include:

1. Not having a long enough clock pulse.
2. Unbuffered outputs
3. Relative strengths of feedback vs. feedforward paths

Print the schematic of your circuit, the test environment, and a plot showing the CLKin, Din, and Qout waveforms.

Deliverables

Turn in the following:

1. The transistor-level schematics of your latch or flop circuit.
2. The schematic of the test environment.
3. The waveform plots showing the cell functioning properly

You must provide hard-copy; electronic submissions will not be accepted.

Be aware that if you choose to work in a team that you are both responsible for knowing how to use all the tools. There will be exam questions which cover tool usage.