Lab #1: Schematic capture
ECEn 451
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In this lab you will use the Cadence tools to create transistor-level schematics implementing a logic function using static CMOS gates; multiple gates may be required. In the next lab, you will create a layout for the function.

For this lab, you will work in teams of either one or two members. Each team must choose one of the following functions to work on:

- a static CMOS 2:1 multiplexer
- an OAI gate with at least 4 inputs
- a minority gate $\overline{AB+BC+AC}$
- an XNOR3 gate

Use 1.8u as the width of the nmos transistors and 5.4u as the width of the pmos transistors.

You may not assume any inverted inputs; in other words, if you need inverters, you should include their transistors in the schematic. The first two Cadence tutorials at http://www.et.byu.edu/groups/ece451web/cadence-help/index.html describe how to set up Cadence and how to use the schematic editor.

Deliverables

Turn in the following:

1. A transistor-level schematic of the logic circuit plotted from Cadence, clearly labeled with the name of the function and its boolean representation.

Be aware that if you choose to work in a team that you are both responsible for knowing how to use all the tools. There will be exam questions which cover tool usage.